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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WANG, JIN CHENG	

ART UNIT	PAPER NUMBER
2672	11

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/722,663	FOULADI ET AL.	
	Examiner	Art Unit	
	Jin-Cheng Wang	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment filed on 02/25/2004 has been entered. Claim 1 has been amended. Claims 1-23 are pending in the application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-10, 12, 15-16, 18, 21 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen U.S. Pat. No. 6,532,018 (hereinafter Chen).

3. Claim 1:

Chen teaches a graphics system, including:

A main processor (See Figure 1 and column 5, lines 34-45);

A graphics coprocessor having an embedded frame buffer (The rasterizer chip 16 and M0-M15 of Figure 1 constitutes the graphics coprocessor or the DRAM graphics coprocessor; see also column 3, lines 4-19); and

A copy pipeline on said graphics coprocessor which transfers data from the embedded frame buffer (the embedded frame buffer of Figure 3 within the graphics coprocessor) to an

external image storage location (the external image storage location such as the *display memory chip 18 of Figure 1* or any "external" image storage location such as *the texture memory 124 of Figure 3* or registers/buffers external to and other than the embedded frame buffer. See Figures 1-3; column 2; column 4, lines 48-67; column 5, lines 1-12);

Wherein the copy pipeline converts that data from one format to another format after reading the data from the embedded frame buffer and during transfer of (e.g., column 3, lines 20-42) prior to writing the data to the external image storage location (e.g., column 2, lines 28-49; column 3, lines 4-42; column 4, lines 48-67; column 5, lines 1-12).

Claim 2:

The claim 2 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the external location being a main memory of the graphics system. However, Chen further discloses the claimed limitation of the external location being a main memory of the graphics system (e.g., Figures 1-3; column 2, lines 28-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 3:

The claim 3 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the copy pipeline being operable to selectively transfer the data to either a display buffer or a texture buffer. However, Chen further discloses the claimed limitation of the copy pipeline being operable to selectively transfer the data to either a display buffer or a texture buffer (e.g., Figures 1-3; column 2, lines 28-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 4:

The claim 4 encompasses the same scope of invention as that of claim 3 except additional claimed limitation of the copy pipeline converting the data to a display format if the data is transferred to the display buffer and a texture format if the data is transferred to the texture buffer. However, Chen further discloses the claimed limitation of the copy pipeline converting the data to a display format if the data is transferred to the display buffer and a texture format if the data is transferred to the texture buffer (e.g., Figures 1-3; column 2, lines 28-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 5:

The claim 5 encompasses the same scope of invention as that of claim 3 except additional claimed limitation that the graphics system further includes a graphics pipeline, wherein the graphics pipeline is operable to use the data in the texture buffer during a rendering process.

However, Chen further discloses the claimed limitation that the graphics system further includes a graphics pipeline, wherein the graphics pipeline is operable to use the data in the texture buffer during a rendering process (e.g., Figures 1-3 and column 1, lines 30-47).

Claim 6:

The claim 6 encompasses the same scope of invention as that of claim 1 except additional claimed limitation that the copy pipeline selectively reads data from the embedded frame buffer in RGB color format or YUV color format. However, Chen further discloses the claimed limitation that the copy pipeline selectively reads data from the embedded frame buffer in RGB color format or YUV color format (e.g., Figures 1-3; figure 4a-4b; column 2, lines 43-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 7:

The claim 7 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of the copy pipeline converting the data from the embedded frame buffer to either a display format or a texture format. However, Chen further discloses the claimed limitation of the copy pipeline converting the data from the embedded frame buffer to either a display format or a texture format (e.g., Figures 1-3; figure 4a-4b; column 2, lines 43-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 8:

The claim 8 encompasses the same scope of invention as that of claim 7 except additional claimed limitation that the copy pipeline writes the data to a display buffer when the data is converted to a display format and the copy pipeline writes the data to a texture buffer when the data is converted to a texture format. However, Chen further discloses the claimed limitation that the copy pipeline writes the data to a display buffer when the data is converted to a display format and the copy pipeline writes the data to a texture buffer when the data is converted to a texture format (e.g., Figures 1-3; figure 4a-4b; column 2, lines 43-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 9:

The claim 8 encompasses the same scope of invention as that of claim 7 except additional claimed limitation of the display buffer and the texture buffer being located in a main memory of the graphics system. However, Chen further discloses the claimed limitation of the display buffer and the texture buffer being located in a main memory of the graphics system (e.g., Figures 1-3; figure 4a-4b; column 2, lines 43-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 10:

The claim 10 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of the graphics pipeline selectively converting the data read from the embedded frame buffer to a YUV color format or an RGB color format. However, Chen further discloses the claimed limitation of the graphics pipeline selectively converting the data read from the embedded frame buffer to a YUV color format or an RGB color format (e.g., Figures 1-3; figure 4a-4b; column 2, lines 43-49; column 4, lines 48-67; column 5, lines 1-12).

4. Claim 12:

Chen teaches a method of transferring data from a graphics chip to an external image storage destination, including:

Storing image data in an embedded frame buffer of the graphics chip (e.g., Figures 1-3; column 2, column 3, lines 4-19); and

Initiating a copy out operation for transferring data from the embedded frame buffer to the external image storage destination (e.g., Figures 1-3; column 2-3, column 4, lines 48-67; column 5, lines 1-12);

Converting the data from one format to another format during the copy out operation (e.g., Figures 1-3; figure 4a and 4b; column 2, lines 28-49; column 4, lines 48-67; column 5, lines 1-12); and

Writing the converted data to the external image storage destination (e.g., Figures 1-3; figure 4a and 4b; column 2, lines 28-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 15:

The claim 15 encompasses the same scope of invention as that of claim 12 except additional claimed limitation that the converting step includes converting the data to a texture format, and the writing step includes writing the texture format data to a texture buffer. However, Chen further discloses the claimed limitation that the converting step includes converting the data to a texture format, and the writing step includes writing the texture format data to a texture buffer (e.g., Figures 1-3; figure 4a-4b; column 2, lines 43-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 16:

The claim 16 encompasses the same scope of invention as that of claim 12 except additional claimed limitation that the converting step includes converting the data to a display format, and the writing step includes writing the texture format data to a display buffer. However, Chen further discloses the claimed limitation that the converting step includes converting the data to a display format, and the writing step includes writing the texture format data to a display buffer (e.g., Figures 1-3; figure 4a-4b; column 2, lines 43-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 18:

The claim 18 encompasses the same scope of invention as that of claim 12 except additional claimed limitation that the writing step includes selectively writing the data to either a display buffer or a texture buffer in a main memory of the graphics system. However, Chen further discloses the claimed limitation that the writing step includes selectively writing the data to either a display buffer or a texture buffer in a main memory of the graphics system (e.g., Figures 1-3; figure 4a-4b; column 2, lines 43-49; column 4, lines 48-67; column 5, lines 1-12).

Claim 21:

The claim 21 encompasses the same scope of invention as that of claim 12 except additional claimed limitation of performing an anti-aliasing operation on the data prior to writing the data to the external image storage destination. However, Chen further discloses the claimed limitation of performing an anti-aliasing operation on the data prior to writing the data to the external image storage destination (e.g., column 5, lines 25-35).

Claim 23:

The claim 23 encompasses the same scope of invention as that of claim 12 except additional claimed limitation of performing RGB color format to another RGB color format. However, Chen further discloses the claimed limitation of performing RGB color format to another RGB color format (e.g., column 6, lines 1-25).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 11, 13, 14, 17, 19, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen U.S. Pat. No. 6,532,018 (hereinafter Chen) as applied to claim 1 and 12 above, and further in view of Nally et al. U.S. Patent No. 5,506,604 (hereinafter Nally) and Nakamura et al. U.S. Patent No. 6,384,831 (hereinafter Nakamura).

7. Claims 11, 13, 14, 17, 19, 20 and 22:

(1) Chen has taught the claim limitation as recited in claims 1 and 12.

(2) However, it is silent on converting the image data from YUV color format to RGB color format or vice versa; the display format being a YUV 4:2:2 format and performing a scaling/gamma correction/de-flickering operation on the image data.

(3) However, Nally teaches converting the image data from YUV color format to RGB color format or vice versa; the display format being a YUV 4:2:2 format and performing a scaling operation on the image data (Nally column 5, lines 1-67; column 6, lines 1-59) and performing a de-flickering/gamma correction operation on the image data (Nakamura the abstract).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the Nally and Nakamura's teachings into the Chen's method and system of transferring data from a graphics chip to an external image storage location because Chen suggests a display chip which directs the rasterizer chip what data to retrieve from the frame buffer and provides some formatting of the data before sending it to be display on a monitor (Chen column 2, lines 30-50) and therefore suggesting an obvious modification.

(5) Therefore, it would have been obvious to have incorporated Nally's decoding and encoding circuitry because it facilitates logic for color conversion from scaling/zooming of the incoming video and graphics data in the frame buffer and Nakamura's image processing operation so that desired image effect can be obtained.

Remarks

8. Applicant's arguments, filed 02/25/2004, paper number 9, have been fully considered but they are not deemed to be persuasive.

9. Applicant argues in essence with respect to the amended Claim 1 and similar claims that:

> "...However, the disclosure relied on by the Examiner only disclose copying data to different locations within the same chip, rather than from an embedded frame buffer on a graphics co-processor to an external memory location, such as main memory of the graphics system."

This is not found persuasive because the claim limitation calls for "an external memory location" rather than "a main memory of the graphics system". Applicant failed to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Moreover, an external memory location can be interpreted as any memory location *external* to the embedded frame buffer or the graphics coprocessor. Since *the display memory chip 18 of Fig. 1* is a memory location external to the embedded frame buffer and the graphics coprocessor, the display memory chip 18 of Fig. 1 meets the claim limitation of the external image memory location. Moreover, the Examiner further asserts that *the texture memory 124 of Figure 3* also meets the claim limitation of "an external image storage location".

The texture memory 124 of Figure 3 and the display memory chip 18 of Figure 1 in the cited reference are both *external* to the embedded frame buffer of Figure 3. Therefore, the cited reference meets the claim limitation of copying data from an embedded frame buffer on a graphics co-processor to an external memory location (See Figures 1-3, column 2-5). It can be clearly understood from the Chen's reference. In column 2 of the cited reference, it is stated "the rasterizer chip 16 is coupled to a plurality of combined memory and logic chips 10 which

provide texture memory and frame buffering. The rasterizer chip 16 is also coupled to display chip 18 which directs the rasterizer chip 16 what data to retrieve from the frame buffer and provides some formatting of that data before sending it to be displayed on a monitor 20." In column 4 of the cited reference, it is stated "the described M chip memory organization permits very fast copying of data from frame buffer memory to texture memory."

10. Applicant argues in essence with respect to the amended Claim 1 and similar claims that:

> "However, the conversion of data identified by the examiner in Chen is done by the rasterizer chip 16, which provides some formatting of the data from the frame buffer prior to sending it to the monitor 20. None of the teachings of Chen cited by the Examiner teach the copy out feature of claim 1, as amended herein, in which the copy pipeline converts the data from one format to another format after reading the data from the embedded frame buffer of a graphics co-processor and during transfer of the data to the external image storage location, such as main memory."

This is not found persuasive because the texture memory 124 of Figure 3 and the display memory chip 18 of Figure 1 in the cited reference are both ***external*** to the embedded frame buffer of Figure 3. Therefore, the cited reference meets the claim limitation of copying data from an embedded frame buffer on a graphics co-processor to an external memory location (See Figures 1-3, column 2-5). It can be clearly understood from the Chen's reference. In column 2 of the cited reference, it is stated "the rasterizer chip 16 is coupled to a plurality of combined memory and logic chips 10 which provide texture memory and frame buffering. The rasterizer chip 16 is also coupled to display chip 18 which directs the rasterizer chip 16 what data to

retrieve from the frame buffer and provides some formatting of that data before sending it to be displayed on a monitor 20." In column 4 of the cited reference, it is stated "the described M chip memory organization permits very fast copying of data from frame buffer memory to texture memory."

Finally, the column 3 of the cited reference also describes the claim limitation of the copy pipeline converts the data from one format to another format after reading the data from the embedded frame buffer of a graphics co-processor and during transfer of the data to the external image storage location.

Therefore, Chen fulfills the amended Claim 1 as currently drafted.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (703) 605-1213. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (703) 305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jcw

JEFFERY BRIER
PRIMARY EXAMINER